IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Applicant:	§	
	§	
A. MORGENSHTEIN et al	§	
	§	
Serial No.: 10/648,474	§	
	§	
Filed: August 27, 2003	§	Group Art Unit: 2819
	§	
For: Logic Circuit and Method of Logic Circuit Design	§	Attorney Docket: 26327
	§	
Examiner:	§	

Commissioner for Patents
PO Box 1450
Alexandria, VA 22313-1450

INFORMATION DISCLOSURE STATEMENT

Sir:

Enclosed is a PTO Form 1449 which lists citations which may be material to the patentability and examination of the above identified application. Also enclosed are copies of the references cited. These are submitted in compliance with the duty of disclosure defined in 37 CFR 1.56. The Examiner is requested to make these citations of official record in this application.

This Information Disclosure Statement under 37 CFR 1.56 is not to be construed as a representation that a search has been made, that additional matter which is material to the examination of this application does not exist, or that any or more of these citations constitutes prior art.

Respectfully submitted,

Sol Sheinbein
Registration No. 25,457

Date: March 30, 2004

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PTO/SB/08A (10-96)

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INFORMATION DISCLOSURE STATEMENT BY APPLICANT

(use as many sheets as necessary)

Complete if Known	
Application Number	10/648,474
Filing Date	August 27, 2003
First Named Inventor	Morgenshtein
Group Art Unit	2819
Examiner Name	
Attorney Docket Number	26327

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U.S. PATENT DOCUMENTS

Examiners Initials	Cite No. [1]	U.S. Patent Document Number	Kind Code[2] (if known)	Name of Patentee or Applicant of Cited Document	Date of Publication of Cited Document MM-DD-YYYY	Pages, columns, lines, Where Relevant Passages or Relevant Figures Appear
		6,486,708		Yamashita et al	11-26-2002	
		6,124,736		Yamashita et al	09-26-2000	
		6,185,719		Sako	02-06-2001	

FOREIGN PATENT DOCUMENTS

Examiners Initials	Cite No. [1]	Foreign Patent Documents Office[3]	Number[4]	Kind Code[5] (if known)	Name of Patentee or Applicant of Cited Document	Date of Publication of Cited Document MM-DD-YYYY	Pages, columns, lines, Where Relevant Passages or Relevant Figures Appear	T[6]

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Examiner Initials	Cite No.[1]	OTHER PRIOR ART – NON PATENT LITERATURE DOCUMENTS Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial symposium, catalog, etc.) date, page(s), volume-issue number(s), publisher, city and/or country where published.	T[2]
		Al-Assadi et al, "Pass-Transistor Logic Design", *Int. J. Electronics*, 70(4):739-749, 1991	
		Chandrakasan et al, "Minimizing Power Consumption in Digital CMOS Circuits", *Proc. IEEE*, 83(4):498-523, 1995	
		Ozdag et al, "High-Speed QDI Asynchronous Pipelines", *Proc. 8th Int. Symposium on Asynchronous Circuits and Systems*, April, 2002	
		Morgenshtein et al, "Gate-Diffusion Input (GDI) – A Novel Power Efficient Method for Digital Circuits: A Design Methodology", *14th Annual IEEE International ASIC/SOC Conference*, Sept., 2001	
		Morgenshtein et al, "Gate-Diffusion Input (GDI): A Power Eficient Method for Digital Combinatorial Circuits", *IEEE Trans. VLSD Systems*, 10(5):566-581, Oct., 2002	
		Morgenshtein et al, "Asynchronous **exagerate** Gate-Diffusion Input (GDI) Circuits", *ISCAS 2002 IEEE International Symposium on Circuits and Systems*, May, 2002	
		David et al, "An Efficient Implementation of Boolean Functions as Self-Timed Circuits", *IEEE Trans. On Computers*, 41(1):2-11, 1992	
		Alidina et al, "Precomputation-Based Sequential Logic Optimization for Low Power", *IEEE Trans. VLSD Systems*, 2(4):426-436, 1994	
		Zimmerman et al, "Low-Power Logic Styles: CMOS Versus Pass-Transistor Logic", *IEEE J. Solid-State Circuits*, 32(7):1079-1090, 1997	
		Yano et al, "Top-Down Pass-Transistor Logic Design", *IEEE J. Solid-State Circuits*, 31(6):792-803, 1996	
		Chandrakasan et al, "Low-Power CMOS Digital Design", *IEEE J. Solid-State Circuits*, 27(4):473-484, 1992	

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